FLORIDA POLYTECHNIC UNIVERSITY

Course Syllabus

Course Information

- **Course Number and Title**: CDA 4210 – VLSI Design
- **Credit Hours:** 3 Credits – (3 Lectures/week)
- **Academic Term:** Spring 2026

Instructor Information

- **Instructor:** Dr. Muhammad Ullah
- **Office Location:** IST 2095
- **Office Hours**: MWF 11:00 am – 12:00 pm or just stop by if not busy, or unavailable, contact the instructor for a mutually convenient time
- **Email address**: mullah@floridapoly.edu

Course Delivery and Course Description

- **Delivery Mode**: In Person (Section – 01: MWF 2:00 pm-2:50 pm (IST-1028))
- **Course Website**: Canvas
- **Official Catalog Course Description**: Topics discussed in this course include CMOS technology, MOSFET timing analysis, dynamic clocked logic, and layout design rules. Digital VLSI chip design is introduced. Computer-aided design software tools and elementary circuit design will be used. Cell library construction.
    - **Course Prerequisites**: EEL 4768 Computer Architecture and Organization
    - **Course Co-requisite**: EEE 3310 Digital Electronics
    - **Communication/Computation Skills Requirement (6A-10.030)**: N
- **Required Texts and Materials:**
    - Required textbook: Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic. Digital Integrated Circuits: A Design Perspective. Second Edition, Pearson, 2003. ISBN: 0130909963.

    - Required Equipment and materials: Scientific calculators, MATLAB tools
      Note: Only use of the following calculator models as used on the Fundamentals of Engineering (FE) Exam will be allowed:
      Casio: All fx-115 and fx-991 models (Any Casio calculator must have "fx-115" or "fx-991" in its model name.)
      Hewlett Packard: The HP 33s and HP 35s models, but no others
      Texas Instruments: All TI-30X and TI-36X models (Any Texas Instruments calculator must have "TI-30X" or "TI-36X" in its model name.)

Course Objectives and Outcomes

- **Course Objectives**:
  - Provide a theoretical and practical background in high-speed VLSI integrated circuits, along with the engineering analytical and design skills.
  - Study the principles of CMOS operation, static and dynamic combinational and sequential circuits design, Semiconductor memory and arithmetic building block design from system perspective.
  - Computer-aided analysis and design of very large scale integrated (VLSI) system will be emphasized.
- **Course Learning Outcomes**:
  - After successfully completing the course with a grade of C (2.0/4.0) or better, the student should be able to do the following Learning Outcomes of Instruction:

#	CLOs	Learning Level	ABET Criteria
1	Explain the fundamental science behind the evolution, compelling issues, measurement of the quality metrics of integrated circuits and the basic concepts related to complementary MOSFET (CMOS) based digital integrated circuits	Understanding (2)	1
2	Explain the Physical Structure and Fabrication process of Integrated Circuits.	Understanding (2)	1
3	Design and synthesize of CMOS and advanced Logic principles based Static and Dynamic Combinational logic circuits	Synthesis (5)	1, 7
4	Design and synthesize of CMOS and advanced Logic principles based Static and Dynamic Sequential logic circuits	Synthesis (5)	1, 7
5	Analyze the timing issues and examine the arithmetic building blocks, memory, and array structures of digital systems	Analyze (4)	1, 7

Note:

ABET 1 - an ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.

ABET 7 - an ability to acquire and apply new knowledge as needed, using appropriate learning strategies

Academic Support Resources

- **Library**: Students can access the Florida Polytechnic University Library through the University website and Canvas, on and off campus. Students may direct questions to library@floridapoly.edu.
- **Tutoring and Learning Center**: The Tutoring and Learning Center (The TLC) provides tutoring to all Florida Poly students who may need additional academic support. The TLC is staffed by students who have excelled in the courses they tutor. They offer support by reviewing concepts and materials from class, clarifying points of confusion and providing assistance with learning strategies. While the focus of TLC is to provide support to students in freshman-level courses, upper-level courses are also tutored at the Center. The TLC is located in the IST Commons (second floor).
- **Knack Tutoring**: Students looking for additional assistance outside of the classroom are advised to consider working with a peer tutor through Knack. Florida Polytechnic University has partnered with Knack to provide students with access to verified peer tutors who have previously aced this course. To view available tutors, visit floridapoly.joinknack.com and sign in with your student account.
- **Academic Success Coaches**: All students at Florida Poly are assigned an Academic Success Coach. Your Academic Success Coach can assist you with academic success strategies. Please visit the Student Success Center on the second floor of the IST building to meet with an Academic Success Coach.

- **Writing Center**: Located on the second floor of the IST (2059/2061), the Writing Center helps students to develop their writing and presentation skills. Consultations are available in person and virtually. For more detail, visit floridapoly.edu/writing center.

Civility and Collegiality (optional statement)

Faculty and students come to the university for the same reason, which is to participate in a highly professional educational environment. To that end, both students and faculty are expected to treat each other with mutual regard and civility. Communication, written, oral and behavioral, between faculty and students must remain respectful. Within and outside of the classroom, students must refrain from derogatory comments toward the faculty member and their fellow students, and faculty as well must refrain from derogatory comments toward their students. Faculty and students should address each other with respect, in accordance with the wishes of the faculty and the students: for example, no one should be addressed by their last name alone.

Faculty from the outset of a course can and should specify what constitutes activities and behavior that take away from, that diminish, the educational environment. An individual student's distracting behavior impedes the education of fellow students, which itself is a form of disrespect. Civility and collegiality also include respecting each other's time: for example, neither students nor faculty should arrive late to class (unless unforeseen, pressing circumstances prevail); faculty should be present at the posted office hours; and students and faculty should be punctual when meeting times are scheduled. In more general terms, collegiality means respecting the right of both faculty and students to participate fully and fairly in the educational enterprise.

Course Policies

Attendance

Students in **face-to-face (this includes labs and C-courses)** courses are expected "to attend all of their scheduled University classes and to satisfy all academic objectives as defined by the instructor" (University Policy, FPU-5.0010AP). Exceptions to any attendance requirements may be made on a case-by-case basis

Participation

Students are expected to participate in the classroom experience. The use of earbuds/headphones during class is specifically not allowed and students who engage in this behavior may be asked to leave the class for the day (noting exceptions for authorized accommodations). In addition, students who routinely do not bring materials to class that are required for participation, will not be given credit for class attendance, and if this becomes a pattern of behavior, may be asked to leave the class for the day. Persistent problems with participation may result in a code of conduct referral.

Late Work/Make-up work

No makeup tests or quizzes, except in case of emergency, e.g., illness and accident. For makeup tests, medical certificate is required, and the instructor must be notified in advance of the test.

Grading Scale

59	60	70	76	80	83	86	90	93
F	D	C	C+	B-	B	B+	A-	A

(See also University Grading Policy).

Percentages that fall between grades will be rounded up.Grades will be posted to Canvas for reference only, and students should make sure they are recorded correctly.

Grades for each assignment will be posted to Canvas and students should make sure they are recorded correctly. However, there is no guarantee that the percentages or projected grades provided there are correct.
The instructor will calculate final percentages and will determine final grades regardless of Canvas calculations.

Assignment/Evaluation Methods

Category	Points
Attendance	5%
Homework, Project and Design Assignment	40%
Quiz	10%
Exams (Exam – I, Exam – II, Exam – III)	45%
Total	**100%**

University Policies

Reasonable Accommodations
The University is committed to ensuring equal access to all educational opportunities. The Office of Disability Services (ODS), facilitates reasonable accommodations for students with disabilities and documented eligibility. It is the student's responsibility to self-identify as a student with disabilities and register with ODS to request accommodations. If you have already registered with ODS, please ensure that you have requested an accommodation letter for this course through the ODS student portal, and communicate with your instructor about your approved accommodations as soon as possible. Arrangements for testing accommodations must be made in advance. Accommodations are not retroactive. If you are not registered with ODS but believe you have a temporary health condition or permanent disability requiring an accommodation, please contact ODS as soon as possible: DisabilityServices@floridapoly.edu; (863) 874-8770; www.floridapoly.edy/disability.

Accommodations for Religious Observances, Practices and Beliefs
The University will reasonably accommodate the religious observances, practices, and beliefs of individuals in regard to admissions, class attendance, and the scheduling of examinations and work assignments. (See University Policy.)

Title IX
Florida Polytechnic University is committed to ensuring a safe, productive learning environment on our campus that prohibits sex discrimination and sexual misconduct, including sexual harassment, sexual assault, dating violence, domestic violence and stalking. Resources are available if you or someone you know needs assistance. Any faculty or staff member you speak to is required to report the incident to the Title IX Coordinator. Please know, however, that your information will be kept private to the greatest extent possible. You will not be required to share your experience. If you want to speak to someone who is permitted to keep your disclosure confidential, please seek assistance from the Florida Polytechnic University Ombuds Office, BayCare's Student Assistance Program, 1-800-878-5470 and locally within the community at Peace River Center, 863-413-2707 (24-hour hotline) or 863-413-2708 to schedule an appointment. The Title IX Coordinator is available for any questions to discuss resources and options available.

Academic Integrity
Violations of academic integrity regulation include actions such as cheating, plagiarism, use of unauthorized resources (including but not limited to use of Artificial Intelligence tools), illegal use of intellectual property, and inappropriately aiding other students. Such actions undermine the central mission of the university and negatively impact the value of your Florida Poly degree. Suspected violations will be fully investigated, possibly resulting in sanctions up to and including expulsion from the university.

Recording Lectures
Students may, without prior notice, record video or audio of a class lecture for a class in which the student is enrolled for their own personal educational use. Recordings may not be used as a substitute for class participation or class attendance. Recordings may not be published or shared in any way, either intentionally or accidentally, without the written consent of the faculty member. Failure to adhere to these requirements is a violation of state law (subject to civil penalty) and the student code of conduct (subject to disciplinary action). *Recording class activities including, but not limited to, lab sessions, student presentations (whether individually or part of a group), class discussion (except when incidental to and incorporated within a class lecture), and invited guest speakers is* ***prohibited****.*

Course Schedule

Week	Date	Topics	Classes	Quiz	Assignment
1.	Jan 12 - 18	Read course syllabus and familiarize with CANVAS. Background of Integrated Circuits: Concepts, Issues and Complexities	3		
2.	Jan 19 – 25	Background of Integrated Circuits: Concepts, Issues and Complexities	2	1	HW - 1
3.	Jan 26 – Feb 1	Properties of Semiconductor Devices: Diode and MOSFET	3	2	HW - 2
4.	Feb 2 – 8	Physical Structure and Fabrication Process of Integrated Circuits	3	3	HW - 3
5.	Feb 9 - 15	CMOS Inverter- Basic building block of integrated circuits	3	4	
6.	Feb 16 – 22	Static Combinational Circuits Designs	3	5a	HW - 4
7.	Feb 23 – Mar 1	Dynamic Combinational Circuits Designs	3	5b	**Exam - I**
8.	Mar 2 - 8	Static Sequential Circuit Designs	3	6a	HW - 5
9.	Mar 9 – 15	Dynamic Sequential Circuit Designs	3	6b	HW - 6
10.	Mar 16 – 22	**Spring Break – No Classes**	0		
11.	Mar 23 - 29	Timing Issues in Digital VLSI Circuits	3	7	HW - 7
12.	Mar 30 – Apr 5	Design from System Perspectives: Arithmetic Building Block	3		
13.	Apr 6 – 12	Design from System Perspectives: Arithmetic Building Block Contd.	3		HW - 8 **Exam - II**
14.	Apr 13 – 19	Design from System Perspectives: Arithmetic Building Block Contd.	3	8	
15.	Apr 20 – 26	Design from System Perspectives: Semiconductor Memory and Array Structures	3		HW - 9
16.	Apr 27 – 28	Design from System Perspectives: Semiconductor Memory and Array Structures Contd.	1	9	HW - 10
	April 29 – May 1, 2026	Reading Days – No Classes	0		Final Project
	May 4 - 8, 2026	Final Exams Days	0		**Exam III**
		Total	**42**		

Note: This is a tentative schedule. Changes may occur as the semester progresses.

WITHTHDRWAL DATE WITHOUT ACADEMIC PENALTY DEADLINE (W ASSIGNED): April 17, 2026