FLORIDA POLYTECHNIC UNIVERSITY

Course Information

- **Course Number and Title**: EEL 3792C - Computer Engineering Design Lab 2
- **Credit Hours:** 4
- **Academic Term:** Spring 2026

Instructor Information

- **Instructor:** Mohammad Farmani
- **Office Location:** BARC-1102
- **Office Hours**: Mondays 10:00 am – 1:00 pm, Tuesdays & Thursdays 10:00 am – 11:00 am.
- **Email address**: mfarmani@floridapoly.edu

Course Delivery and Course Description

- **Delivery Mode**: All class meetings are in person and on campus unless pre-announced otherwise for specific days. It is important for students to attend so they can participate in the discussion; lectures will be used to present new topics each week and to have a broad engineering design related discussion.
- **Course Website**: Canvas Link

Official Catalog Course Description: THIS COURSE IS A CONTINUATION OF COMPUTER ENGINEERING LAB DESIGN 1. STUDENTS WILL BE REASSEMBLED INTO TEAMS AND TASKED WITH REVERSE ENGINEERING AND REFINING PREVIOUSLY CREATED ALPHA PROTOTYPE DEVICES OR SYSTEMS. AFTER REFINEMENT STUDENT TEAMS WILL PERFORM TESTING ALONG WITH SIMULATION, VERIFICATION, AND VALIDATION OF THEIR PROJECTS. TEAMS WILL THEN ENGAGE IN PEER-TO-PEER LEARNING WITH OTHER LABORATORY GROUPS AND EVENTUALLY CYCLE THROUGH ALL THE STUDENT GENERATED LABORATORY EXERCISES IN MICROPROCESSORS, COMPUTER ARCHITECTURE AND ORGANIZATION, AND DATA STRUCTURES AND ALGORITHMS AND OTHER PROJECT BASED LEARNING ACTIVITIES SUPPORTING COMPUTER ENGINEERING APPLICATIONS.

  - **Course Pre and/or Co-Requisites**: EEL 3791C - Computer Engineering Design Lab 1
  - **Communication/Computation Skills Requirement (6A-10.030)**: N
- **Required Texts and Materials:**
  - FPGA Prototyping by SystemVerilog Examples: Xilinx MicroBlaze MCS SoC Edition, Pong P. Chu, 2nd Edition, Wiley, 2018, ISBN 978-1-119-28266-2
- **Optional / additional references:**
  - Additional readings and resources may be assigned depending on the nature of each project.
- **Required Hardware/Software**
  - Xilinx Spartan 7 XC7S50 FPGA board
  - Xilinx Vivado (WebPACK) design suite
  - Lab peripherals as specified in assignments (e.g., LEDs/switches on board, VGA, audio, UART, etc. as available in the lab)

Course Objectives and Outcomes

Course Objectives:
By the end of the course, students will:

- Apply HDL design, simulation, and synthesis workflows to non-trivial digital systems.
- Implement and debug digital designs on a Spartan-7 FPGA using Vivado.
- Integrate IP cores and build a MicroBlaze-based SoC using the Chu text as a reference.
- Plan, execute, and document a multi-week FPGA project in a small team.

Course Learning Outcomes:
After successfully completing the course with a grade of C (2.0/4.0) or better, the student should be able to do the following Learning Outcomes of Instruction:

#	CLOs	Learning Level	ABET Criteria
1	Design, implement, and analyze the performance of digital systems using SystemVerilog HDLs and modern CAD tools.	Comprehension (2)	1, 6, 7-D
2	Design, implement, and analyze the performance of digital systems on FPGAs, including interfacing with on-board peripherals.	Synthesis (5)	1, 6, 7-D
3	Use modern simulation and FPGA tools (e.g., Vivado) to verify, evaluate, and troubleshoot digital system behavior and performance.	Application (3)	1, 6, 7-D
4	Develop and build a complex FPGA-based system through functional specification, planning, implementation, integration, and comprehensive reporting.	Synthesis (5)	1, 3, 6, 7-D

Academic Support Resources

- **Library**: Students can access the Florida Polytechnic University Library through the University website and Canvas, on and off campus. Students may direct questions to library@floridapoly.edu.
- **Tutoring and Learning Center**: The Tutoring and Learning Center (The TLC) provides tutoring to all Florida Poly students who may need additional academic support. The TLC is staffed by students who have excelled in the courses they tutor. They offer support by reviewing concepts and materials from class, clarifying points of confusion and providing assistance with learning strategies. While the focus of TLC is to provide support to students in freshman-level courses, upper-level courses are also tutored at the Center. The TLC is located in the IST Commons (second floor).
- **Knack Tutoring**: Students looking for additional assistance outside of the classroom are advised to consider working with a peer tutor through Knack. Florida Polytechnic University has partnered with Knack to provide students with access to verified peer tutors who have previously aced this course. To view available tutors, visit floridapoly.joinknack.com and sign in with your student account.
- **Academic Success Coaches**: All students at Florida Poly are assigned an Academic Success Coach. Your Academic Success Coach can assist you with academic success strategies. Please visit the Student Success Center on the second floor of the IST building to meet with an Academic Success Coach.
- **Writing Center**: Located on the second floor of the IST (2059/2061), the Writing Center helps students to develop their writing and presentation skills. Consultations are available in person and virtually. For more detail, visit https://floridapolytechnic.libguides.com/writingservices.

Civility and Collegiality

Faculty and students come to the university for the same reason, which is to participate in a highly professional educational environment. To that end, both students and faculty are expected to treat each other with mutual regard and civility. Communication, written, oral and behavioral, between faculty and students must remain respectful. Within and outside of the classroom, students must refrain from derogatory comments toward the faculty member and their fellow students, and faculty as well must refrain from derogatory comments toward their students. Faculty and students should address each other with respect, in accordance with the wishes of the faculty and the students: for example, no one should be addressed by their last name alone.

Faculty from the outset of a course can and should specify what constitutes activities and behavior that take away from, that diminish, the educational environment. An individual student's distracting behavior impedes the education of fellow students, which itself is a form of disrespect. Civility and collegiality also include respecting each other's time: for example, neither students nor faculty should arrive late to class (unless unforeseen, pressing

circumstances prevail); faculty should be present at the posted office hours; and students and faculty should be punctual when meeting times are scheduled. In more general terms, collegiality means respecting the right of both faculty and students to participate fully and fairly in the educational enterprise.

Course Policies

Attendance

- Students in **face-to-face (this includes labs and C-courses)** courses are expected "to attend all of their scheduled University classes and to satisfy all academic objectives as defined by the instructor" (University Policy, FPU-5.0010AP).
- Attendance at all class meetings is expected. Absence does not excuse a student from material covered or any activity done on that day, nor does it extend a deadline.
- Students should inform the instructor as soon as possible if an absence is expected. The instructor should be contacted as soon as possible if an absence was due to an unforeseen emergency. Documentation may be required in either case.
- Attendance is ***mandatory during presentation days*** (when your team or other teams present). If you are not present during any presentation day you will not receive credit for that presentation milestone (In Class or Panel Presentations).

Email Policy

Emails must be sent from your Florida Poly email account to the Florida Poly email address of the instructor (name@floridapoly.edu). Please allow up to 36 hours on weekdays for a response, after which you may send a follow-up email. Emails must be composed in a professional manner with a greeting, signature, and in an organized fashion. **NO CANVAS Messages.**

Participation

Students are expected to participate in the classroom experience. The use of earbuds/headphones during class is specifically not allowed and students who engage in this behavior may be asked to leave the class for the day (noting exceptions for authorized accommodations). In addition, students who routinely do not bring materials to class that are required for participation, will not be given credit for class attendance, and if this becomes a pattern of behavior, may be asked to leave the class for the day. Persistent problems with participation may result in a code of conduct referral.

Late Work/Make-up work

Late work is generally not accepted unless the student or team has communicated and come to an agreement with the instructor in advance.

Grading Scale

Grade	Percentage
A	100 – 90
A-	89 – 87
B+	86 – 84
B	83 – 80
B-	89 – 77
C+	76 – 74
C	73 – 70
C-	69 – 67
D+	66 – 64

Assignment/Evaluation Methods

Grade items	Points
Lab Reports + Quizzes	50%
Final Project (Demo + PPT)	20%
Final Project (Report)	30%
Total	100%

University Policies

Reasonable Accommodations

The University is committed to ensuring equal access to all educational opportunities. The Office of Disability Services (ODS), facilitates reasonable accommodations for students with disabilities and documented eligibility. It is the student's responsibility to self-identify as a student with disabilities and register with ODS to request accommodations. If you have already registered with ODS, please ensure that you have requested an accommodation letter for this course through the ODS student portal, and communicate with your instructor about your approved accommodations as soon as possible. Arrangements for testing accommodations must be made in advance. Accommodations are not retroactive. If you are not registered with ODS but believe you have a temporary health condition or permanent disability requiring an accommodation, please contact ODS as soon as possible: DisabilityServices@floridapoly.edu; (863) 874-8770; www.floridapoly.edy/disability.

Accommodations for Religious Observances, Practices and Beliefs

The University will reasonably accommodate the religious observances, practices, and beliefs of individuals in regard to admissions, class attendance, and the scheduling of examinations and work assignments. (See University Policy.)

Title IX

Florida Polytechnic University is committed to ensuring a safe, productive learning environment on our campus that prohibits sex discrimination and sexual misconduct, including sexual harassment, sexual assault, dating violence, domestic violence and stalking. Resources are available if you or someone you know needs assistance. Any faculty or staff member you speak to is required to report the incident to the Title IX Coordinator. Please know, however, that your information will be kept private to the greatest extent possible. You will not be required to share your experience. If you want to speak to someone who is permitted to keep your disclosure confidential, please seek assistance from the Florida Polytechnic University Ombuds Office, BayCare's Student Assistance Program, 1-800-878-5470 and locally within the community at Peace River Center, 863-413-2707 (24-hour hotline) or 863-413-2708 to schedule an appointment. The Title IX Coordinator is available for any questions to discuss resources and options available.

Academic Integrity

Violations of academic integrity regulation include actions such as cheating, plagiarism, use of unauthorized resources (including but not limited to use of Artificial Intelligence tools), illegal use of intellectual property, and inappropriately aiding other students. Such actions undermine the central mission of the university and negatively impact the value of your Florida Poly degree. Suspected violations will be fully investigated, possibly resulting in sanctions up to and including expulsion from the university.

Recording Lectures

Students may, without prior notice, record video or audio of a class lecture for a class in which the student is enrolled for their own personal educational use. Recordings may not be used as a substitute for class participation or class attendance. Recordings may not be published or shared in any way, either intentionally or accidentally, without the written consent of the faculty member. Failure to adhere to these requirements is a violation of state law (subject to civil penalty) and the student code of conduct (subject to disciplinary action). *Recording class activities including, but not limited to, lab sessions, student presentations (whether individually or part of a group), class discussion (except when incidental to and incorporated within a class lecture), and invited guest speakers is* ***prohibited****.*

Revisions to the Syllabus

The faculty reserve the right to correct typos or other errors in the syllabus and make other reasonable adjustments to maintain the quality and integrity of the course in response to unanticipated circumstances.

Course Schedule (Tentative)

Week	Activity
1	Course introduction; review of digital design and HDL basics; introduction to SystemVerilog and simulation in Vivado; simple combinational circuits in simulation; confirm tools/board setup (optional short LED demo on FPGA).
2	Sequential logic: flip-flops, registers, counters; basic finite state machines; simulation with simple testbenches; first required FPGA lab: FSM-based controller on the Spartan-7 board.
3	FSMD (finite state machine with datapath) and hierarchical design; lab: FSMD-based PWM or timer (simulate, then implement on FPGA).
4	FPGA memories (block RAM, register files); address decoding and simple memory-mapped interfaces; lab: memory-based design (e.g., lookup table or buffer) on FPGA.
5	Integrating multiple modules (datapath + controller); on-board I/O (LEDs, switches, buttons); lab: multi-peripheral controller design and testing on FPGA.
6	Introduction to FPGA-based SoC concepts; overview of Chu's MicroBlaze-style SoC framework; discuss hardware/software partitioning and toolflow.
7	Minimal SoC lab: processor core with GPIO (LEDs/switches); write a simple C program to interact with the hardware; build and test the complete flow.
8	More advanced peripheral design (e.g., timer or UART-like interface) around the SoC; discussion of final project ideas and constraints; Final Project description and rubric released.
9	Final Project proposals due (teams, problem statement, block diagrams, timeline); in-lab design reviews; start implementing core modules.
10	Spring Break, no class or labs.
11	Final Project, Week 1: implement and simulate core modules; initial synthesis and basic FPGA bring-up; weekly progress check.
12	Final Project, Week 2: integrate major modules; focus on debugging and timing issues on FPGA; weekly progress check.
13	Final Project, Week 3: add remaining features; intermediate in-class demo/checkpoint; continue report and slide preparation.
14	Final Project, Week 4: system-level testing and performance evaluation; finalize design; polish documentation.
15	Final Project, Week 5: final integration and rehearsal; project demos and presentations; submit final reports and code.
16	Buffer week (if applicable): make-ups, extra demos, and course reflection, no new assignments.